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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/796,887	03/08/2004	David Ralph Scheid	David Scheid	2863

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EXAMINER	
DUONG, KHANH B	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 09/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/796,887	SCHEID, DAVID RALPH	
	Examiner	Art Unit	
	Khanh B. Duong	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) *19-25* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,10-12,14 and 16-18* is/are rejected.

7)☒ Claim(s) *6-9,13 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/8/04*.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *8/24/05*.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-18, drawn to a method of forming a semiconductor device, classified in class 438, subclass 109.

II. Claims 19-25, drawn to a semiconductor device, classified in class 257, subclass 678.

The inventions are distinct, each from the other because of the following reasons:

Inventions I and II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case, the device as claimed can alternatively be formed by: (1) attaching a plurality of semiconductor dice directly to the thin film interconnect instead of the substrate, or (2) attaching a plurality of semiconductor dice directly to the thin film interconnect after bending the thin film interconnect.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and the search required for Group II is not required for Group I, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art because of their recognized divergent subject matter, restriction for examination purposes as indicated is proper.

During a telephone conversation with Anthony Bourget on August 24, 2005 a provisional election was made without traverse to prosecute the invention of Group I, claims 1-18. Affirmation of this election must be made by applicant in replying to this Office action. Claims 19-25 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Drawings

The drawings (Figs. 7-10) are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: "82".

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the step of "attaching the bottom sides of the plurality of semiconductor dice to a cavity substrate so that the plurality of semiconductor dice are in adjacent disposition within the large substrate pocket and define one or more bending regions" must be shown or the feature(s) canceled from the claim(s) [see Claim 11, lines 1-4]. No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure

must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

Claims 2, 11, 14-16 and 18 are objected to because of the following informalities:

Re claim 2, line 3, claim 11, lines 5, 7 and 8, claim 14, line 5, claim 15, line 2, and claim 18, line 2, "die" should be "dice".

Re claim 16, line 11, "the folding region" should be --the bending region-- for constancy.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 11 and 15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Re claim 11, the claim recites "the step of attaching the bottom sides of the plurality of semiconductor dice to a cavity substrate" and "the large substrate pocket" in lines 1-3. There are insufficient antecedent basis for these limitations in the claim.

Re claim 15, the claim recites "the dielectric layers" and "the unused sides" on lines 2 and 3. There are insufficient antecedent basis for these limitations in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 11, 12 and 16-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Eichelberger et al. (U.S. Patent No. 5,452,182).

Re claim 1, Eichelberger et al. ("Eichelberger") discloses in FIGs. 3-7 and 19 a method of fabricating integrated circuits from a plurality of semiconductor dice 20, each semiconductor die 20 defining a top side and a bottom side, the method comprising: attaching the bottom sides of the plurality of semiconductor dice 20 to a substrate 14 so that the plurality of semiconductor dice 20 are in adjacent disposition and define one or more bending regions; creating a planar processing area for subsequent seamless high density thin film interconnect 30 on the top sides of the plurality of semiconductor dice 20 and the one or more bending regions so that the plurality of semiconductor dice 20 are electrically interconnected; removing the substrate 14 from the bottom sides of the plurality of semiconductor dice 20; and bending the thin film interconnect 30 at the one or more bending regions so that the semiconductor dice 20 may

overlap to form a stacked plurality of semiconductor dice 20 [see col. 10, line 17 to col. 11, line 52, and col. 16, lines 25-63].

Re claim 2, Eichelberger expressly discloses in FIG. 3 the step of attaching the bottom sides of the plurality of semiconductor dice 20 comprises the step of bonding the bottom sides of the semiconductor die 20 to the substrate 14.

Re claim 3, Eichelberger expressly discloses in FIGs. 4 and 5 the step of creating a planar processing area for subsequent seamless high density thin film interconnect 30 on the top sides of the plurality of semiconductor dice 20 and the one or more bending regions so that the plurality of semiconductor dice 20 are electrically interconnected comprises the step of laminating a sheet of flexible dielectric material (32, 34 & 36) to the top sides of the plurality of semiconductor dice 20.

Re claim 11, Eichelberger expressly discloses in FIG. 5 the step of attaching the bottom sides of the plurality of semiconductor dice 20 to a cavity substrate 14: so that the plurality of semiconductor dice 20 are in adjacent disposition within the cavity substrate 14 and define one or more bending regions comprises the steps of: defining a set of semiconductor die 20 to form a stacked plurality of semiconductor dice 20; and arranging the set of semiconductor die 20 to minimize electrical connections in the thin film interconnect 30, wherein multiple sets of semiconductor die 20 define the plurality of semiconductor dice 20.

Re claim 12, Eichelberger expressly discloses in FIG. 15 the step of creating a pad layer (pads 37) on a section of the thin film interconnect 30, wherein the pad layer is shown in FIG. 4 as overlaying at least one of the plurality of semiconductor dice 20 and is suitable for subsequent flip chip attachment and wire bond assembly.

Re claim 14, Eichelberger expressly discloses in FIG. 1 the step of creating another pad layer wherein the next level connection pads 34 are placed in at least one bending region defined by a die gap and then used for subsequent electrical solder connection within the bent region of the thin film interconnect 30 along the side of the stacked die assembly as shown in FIG. 19.

Re claim 16, see discussion above regarding claim 1. Furthermore, Eichelberger expressly discloses in FIG. 19 the formation of a multidimensional interconnected dice structure by bending the flexible member 30 at the bending regions.

Re claim 17, Eichelberger expressly discloses in FIG. 19 the step of bending comprises the step of bending the flexible member 30 at the die gap regions so that the plurality of semiconductor dice 20 define a geometric volume.

Re claim 18, Eichelberger expressly discloses in FIG. 19 the step of bending at the die gap region defines an angle between the two dice within a range of 0 to 360 degrees.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eichelberger in view of Nicewarner, Jr. et al. (U.S. Patent No. 5,776,797).

Re claim 4, Eichelberger discloses in FIG. 4 the step of creating a thin film interconnect 30 on the top sides of the plurality of semiconductor dice 20 and the one or more folding regions so that the plurality of semiconductor dice 20 are electrically interconnected further comprises the steps of: creating vias ("via holes") through the sheet of flexible material (32, 34 & 36) down to the top sides of the plurality of semiconductor dice 20; depositing a conductive material within the vias; and forming conductive interconnection routes 34 between the vias to create a seamless interconnection interface capable of area array connections [see col. 8, lines 12-16]. However, Eichelberger fails to disclose forming area array connection with pad pitches from 50 to 1,000 microns.

Nicewarner, Jr. et al. ("Nicewarner") suggests forming area array connection with pad pitches from 0.010 to 0.100 of an inch, which is equivalent to 254 to 2,540 microns [see col. 10, lines 42-44].

Since Eichelberger and Nicewarner are from the same field of endeavor, the purpose disclosed by Nicewarner would have been recognized in the pertinent prior art of Eichelberger.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to optimize and select appropriate pad pitches within the range as suggested by Nicewarner. The selection of parameters such as energy, power, concentration, temperature, time, depth, thickness, etc., would have been obvious and involve routine optimization which has been held to be within the level of ordinary skill in the art. "Normally, it is to be expected that a change in temperature, or in concentration, or in both, would be an unpatentable modification. Under some circumstances, however, changes such as these may be impart patentability to a process if the particular ranges claimed produce new and unexpected result which is different in kind and not merely degree from results of prior art ... such ranges are termed 'critical ranges' and the applicant has the burden of proving such criticality ... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation". *In re Aller*, 105 USPQ 233, 235 (CCPA 1955). See also MPEP 2144.05.

Re claim 5, Eichelberger discloses the use of polyimide in forming the flexible interconnect layer 30 [see col. 7, lines 57-66].

Allowable Subject Matter

Claims 6-8, 9, 13 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kornrumpf (U.S. 5,345,205) and Paurus et al. (U.S. 5,448,511) disclose relevant teachings regarding flexible interconnections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh B. Duong whose telephone number is (571) 272-1836. The examiner can normally be reached on 10:00-6:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KBD

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